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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,247	02/17/2004	Lianrui Zhang	TI-36929 (032350.B585)	9664

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,247	ZHANG ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a plurality of phase comparator [claim 21] must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. For examination purposes, the examiner is taking the position that only one phase comparator is claimed.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 5 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa (JP-09181133A).

Regarding claim 5, Hasegawa discloses [see Fig. 1] a method for testing a device, comprising: testing an electronic device (internal circuitry 15) having a first operating frequency by a tester device (tester device 11) having a second operating frequency; during the testing, repeatedly determining [via phase comparator 19] any frequency difference between the first operating frequency and the second operating frequency; for each determination of the frequency difference [via comparator 19], generating [via VOC 21] a voltage value indicative of the frequency difference; and using the generated voltage [via VCO 21] to adjust the first operating frequency [via tester device 11].

Regarding claim 21, Hasegawa discloses [see Fig. 1] a testing system for testing a plurality of integrated circuit devices comprising a tester (tester device 11) having an operating frequency; inherently [see Note below] a board adapted to accommodate a plurality of integrated circuit devices (IC 12) to be tested; a plurality of integrated circuit device under test (DUT (internal circuitry 15) on the board, a plurality of clock circuit (output signal 18, S1 and S2), each generating a operating frequency for a DUT (15); a phase comparator device (phase comparator 19); each phase compactor (19) device having a pair of input terminals [from clock signal 16 and

output S1] adapted to receiving the operating frequency of the tester (11) and the operating frequency of a DUT (15), and an output terminal adapted to transmitting a signal indicative of a difference between the operating frequencies of the tester (11) and the DUT (15); and each clock circuit (18, S1 and S2) including a voltage controlled oscillator (VCO 21) circuit operable to adjust the DUT (15) operating frequency based on the output signal of the phase comparator device (19).

Although the prior art does not specifically disclose the claimed a board, this feature is seen to be an inherent teaching of that device since a integrated circuit is disclosed and it is apparent that some type of board must be presented for the purpose of holding the IC in place while the IC is being tested by the tester as intended.

Regarding claim 22, Hasegawa discloses the comparator device (19) is not affixed on the board [not shown].

Regarding claim 23, Hasegawa discloses a portion of the clock circuit (18, S1 and S2) is embedded in the integrated circuit DUT (15).

Regarding claim 24, Hasegawa discloses the comparator (19) is a part of a PLL circuit, which further comprises a low pass filter (low pass filter 20) and an amplifier (frequency divider 22).

Regarding claim 25, Hasegawa discloses the VCO circuit (21) is coupled to the amplifier (22).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Riggio, Jr. (5596280) and Yamashita (6378098) disclose a method and apparatus for a semiconductor test system.

5. Applicant's arguments with respect to claim 5 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
November 1, 2005